

## Quad buffer/line driver; 3-state

## 74HC/HCT126

### FEATURES

- Output capability: bus driver
- $I_{CC}$  category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT126 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The HC/HCT126 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a HIGH impedance OFF-state.

The "126" is identical to the "125" but has active HIGH enable inputs.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay nA to nY	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	9	11	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per buffer	notes 1 and 2	23	24	pF

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

### ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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## 74HC/HCT126

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY		30	100		125		150	ns	2.0	Fig.6
			11	20		25		30			
			9	17		21		26			
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time nOE to nY		41	125		155		190	ns	2.0	Fig.7
			15	25		31		38			
			12	21		26		32			
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time nOE to nY		41	125		155		190	ns	2.0	Fig.7
			15	25		31		38			
			12	21		26		32			
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14	60		75		90	ns	2.0	Fig.6
			5	12		15		18			
			4	10		13		15			

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per unit, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nOE	1.00

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HCT								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY		14	24		30		36	ns	4.5	Fig.6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time nOE to nY		13	25		31		38	ns	4.5	Fig.7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time nOE to nY		18	28		35		42	ns	4.5	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.6